Claims

[c1] 1. A method of processing a cap wafer configured for mating with a device wafer in the production of a die package, the method comprising the steps of:
providing a semiconductor wafer having first and second oxide layers on oppositely-disposed first and second surfaces, respectively, thereof;
forming first and second masking layers on the first and second oxide layers, respectively;
etching the first and second masking layers to define first and second mask patterns, respectively, the first and second mask patterns exposing regions of the first and second oxide layers, the exposed regions comprising first and second exposed regions of the first oxide layer and first exposed regions of the second oxide layer, the first mask pattern masking third and fourth regions of the first oxide layer and the second mask pattern masking second regions of the second oxide layer, the fourth regions of the first oxide layer being aligned with the second regions of the second oxide layer;
forming an oxide mask on the first and second exposed regions of the first and second oxide layers, the first and second mask patterns preventing the oxide mask from

forming on the third and fourth regions of the first oxide layer and the second regions of the second oxide layer;
removing the first and second mask patterns to expose the third and fourth regions of the first oxide layer and the second regions of the second oxide layer;
removing the third and fourth regions of the first oxide layer and the second regions of the second oxide layer to expose first, second and third surface regions, respectively, of the wafer between portions of the oxide mask;
etching the first, second and third surface regions of the wafer, wherein etching of the first surface regions of the wafer produces recesses in the first surface of the wafer and etching of the second and third surface regions of the wafer produces through-holes in the wafer; and then
removing the oxide mask to yield a cap wafer with multiple through-holes and recesses.

[c2] 2. The method according to claim 1, wherein the first and second masking layers are formed of silicon nitride.

[c3] 3. The method according to claim 1, wherein the wafer is a silicon wafer, the first and second oxide layers are silicon dioxide layers, and the oxide mask is formed of silicon dioxide grown by oxidizing the first and second exposed regions of the first oxide layer and the second exposed region of the second oxide layer.

[c4] 4. The method according to claim 1, further comprising the step of mating the cap wafer with a device wafer so that the recesses of the cap wafer define cavities enclosing micromachined elements on the device wafer, bonding the cap wafer to the device wafer to form a wafer stack, and then singulating die from the wafer stack to produce multiple device packages.

[c5] 5. The method according to claim 4, wherein as a result of the mating step the through-holes provide access to bond pads on the device wafer.

[c6] 6. The method according to claim 1, wherein the step of etching the first, second and third surface regions of the wafer to produce the through-holes and the recesses is an anisotropic etch.

[c7] 7. The method according to claim 1, wherein a surface defect is present in at least one of the first and second mask patterns prior to the step of forming the oxide mask, the step of forming the oxide mask results in oxide forming in the defect, and the step of etching the first, second and third surface regions of the wafer causes the oxide in the defect to be undercut so as not to effect the sizes and shapes of the through-holes or recesses formed in the first, second and third surface regions of the wafer.

[c8] 8. A method of producing a MEMS device package, the method comprising the steps of:
providing a semiconductor wafer having first and second oxide layers on oppositely-disposed first and second surfaces, respectively, thereof;
depositing first and second masking layers on the first and second oxide layers, respectively;
etching the first and second masking layers to define first and second mask patterns, respectively, the first and second mask patterns exposing regions of the first and second oxide layers, the exposed regions comprising first and second exposed regions of the first oxide layer and first exposed regions of the second oxide layer, the first mask pattern masking third and fourth regions of the first oxide layer and the second mask pattern masking second regions of the second oxide layer, the fourth regions of the first oxide layer being aligned with the second regions of the second oxide layer;
growing an oxide mask on the first and second exposed regions of the first and second oxide layers, the first and second mask patterns preventing the oxide mask from forming on the third and fourth regions of the first oxide layer and the second regions of the second oxide layer;
removing the first and second mask patterns to expose the third and fourth regions of the first oxide layer and

the second regions of the second oxide layer;
removing the third and fourth regions of the first oxide layer and the second regions of the second oxide layer to expose first, second and third surface regions, respectively, of the wafer between portions of the oxide mask;
etching the first, second and third surface regions of the wafer, wherein etching of the first surface regions of the wafer produces recesses in the first surface of the wafer and etching of the second and third surface regions of the wafer produces through-holes in the wafer;
removing the oxide mask to yield a cap wafer with multiple through-holes and recesses;
mating the cap wafer with a device wafer so that the recesses of the cap wafer define cavities enclosing micromachined elements on the device wafer and the through-holes provide access to bond pads on the device wafer;
bonding the cap wafer to the device wafer to form a wafer stack; and then
singulating die from the wafer stack to produce multiple device packages.

[c9] 9. The method according to claim 8, wherein the first and second masking layers are formed of silicon nitride.

[c10] 10. The method according to claim 8, wherein the wafer is a silicon wafer, the first and second oxide layers are

silicon dioxide layers, and the oxide mask is formed of silicon dioxide grown by oxidizing the first and second exposed regions of the first oxide layer and the second exposed region of the second oxide layer.

[c11] 11. The method according to claim 8, wherein the step of etching the first, second and third surface regions of the wafer to produce the through-holes and the recesses is an anisotropic etch.

[c12] 12. The method according to claim 8, wherein a surface defect is present in at least one of the first and second mask patterns prior to the step of forming the oxide mask, the step of forming the oxide mask results in oxide forming in the defect, and the step of etching the first, second and third surface regions of the wafer causes the oxide in the defect to be undercut so as not to effect the sizes and shapes of the through-holes or recesses formed in the first, second and third surface regions of the wafer.